389-729

R6551

R6551
Asynchronous Communications Interface Adapter (ACIA)

DESCRIPTION

The Rockwell R6551 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times an external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R6551's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

ORDERING INFORMATION

Part No.: R6551___

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
- Frequency Range:
  - No Letter = 1 MHz
  - A = 2 MHz

FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 or 1 MHz operation
- 5.0 Vdc ± 5% supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 microprocessors

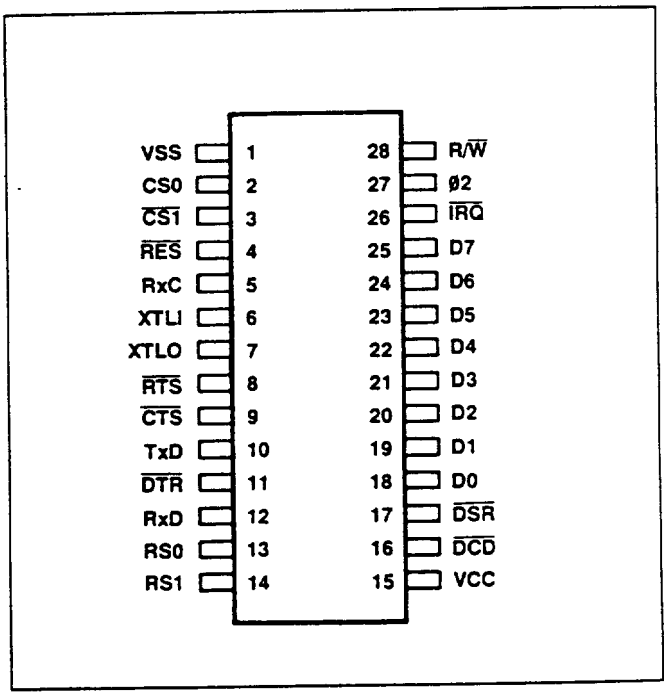


Figure 1. R6551 ACIA Pin Configuration

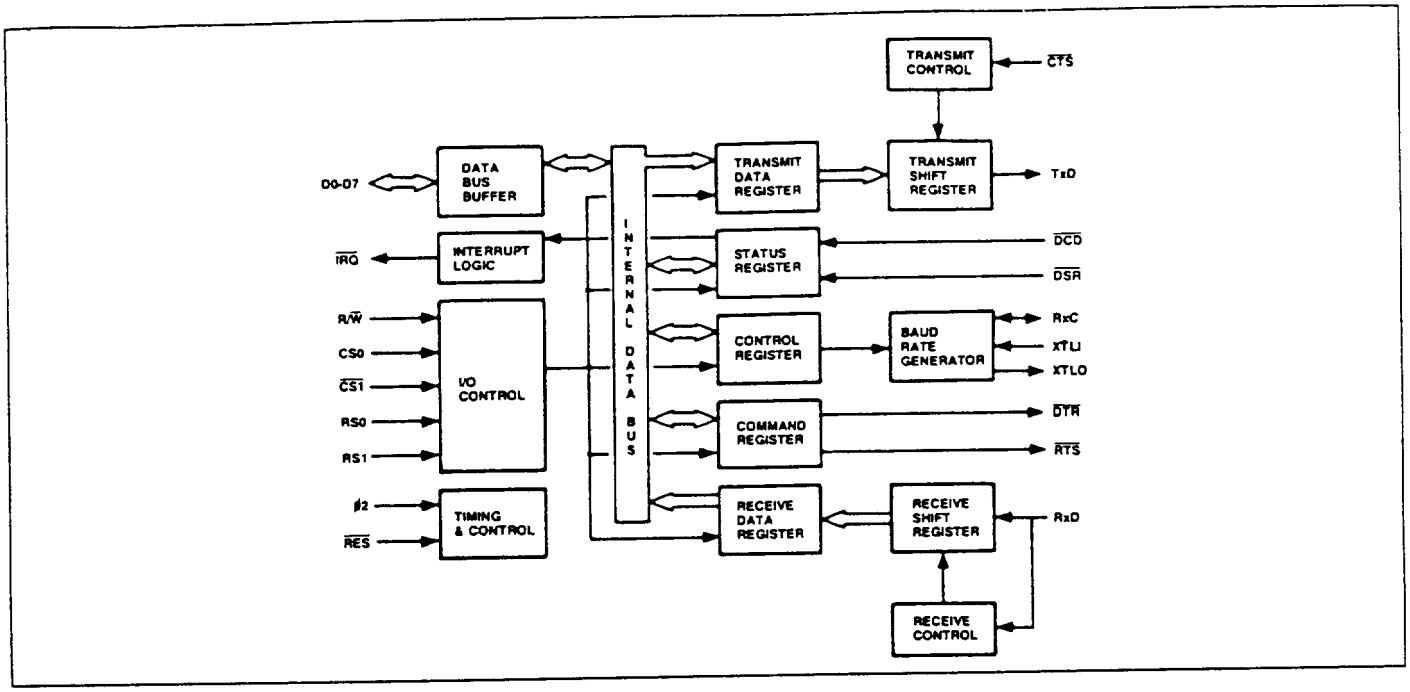


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

A block diagram of the ACIA is presented in Figure 2. A description of each functional element of the device follows.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data lines to the ACIA internal data bus. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer drives the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select (RS1, RS0) and Read/Write (R/$\overline{W}$) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus, the registers, the Data Bus Buffer, the microprocessor data bus, and the hardware reset.

Timing is controlled by the system Ø2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the Ø2 high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmit and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/$\overline{W}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0" Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status information. The interrupt conditions are Data Set Ready and Data Carrier Detect transitions, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRF	OVRN	FE	PE

Bit 7 **Interrupt (IRQ)**
- 0 No interrupt
- 1 Interrupt has occurred

Bit 6 **Data Set Ready ($\overline{DSR}$)**
- 0 $\overline{DSR}$ low (ready)
- 1 $\overline{DSR}$ high (not ready)

Bit 5 **Data Carrier Detect ($\overline{DCD}$)**
- 0 $\overline{DCD}$ low (detected)
- 1 $\overline{DCD}$ high (not detected)

Bit 4 **Transmitter Data Register Empty**
- 0 Not empty
- 1 Empty

Bit 3 **Receiver Data Register Full**
- 0 Not full
- 1 Full

Bit 2 **Overrun***
- 0 No overrun
- 1 Overrun has occurred

Bit 1 **Framing Error***
- 0 No framing error
- 1 Framing error detected

Bit 0 **Parity Error***
- 0 No parity error
- 1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	Hardware reset
—	—	—	—	—	0	—	—	Program reset

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (Bit 2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

NOTE: There is a delay of approximately $\frac{1}{9}$ of a bit time after TDR becomes empty/full before this flag is updated.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until after the Status Register has been interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x External Clock
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
–	–	–	–	–	–	–	–	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $^1/_{16}$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator

If the Receiver clock uses the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

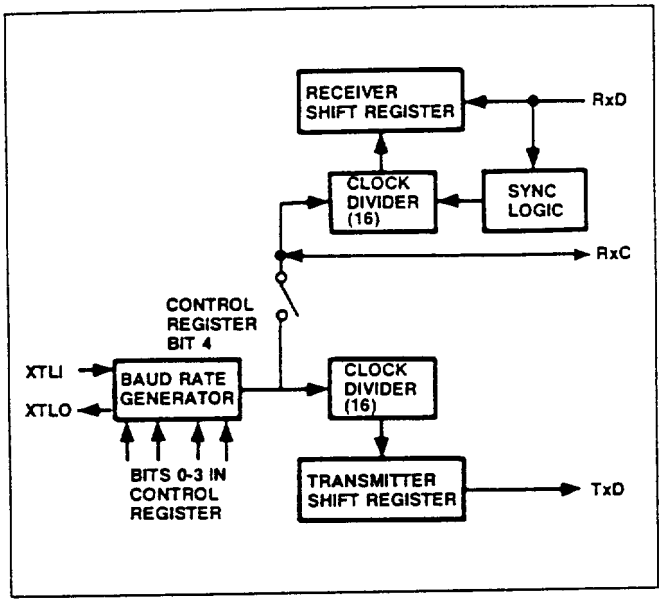


Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $^1/_{16}$ an external clock A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, or 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PMC1	PMC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode Bits 2 and 3 must also be zero for receiver echo mode, $\overline{RTS}$ will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{RTS}$ = High, transmitter disabled*
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, tansmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled, transmit break on TxD**

Bit 1 Receiver Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled (receiver)
1	$\overline{IRQ}$ disabled (receiver)

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)*
1	Data terminal ready ($\overline{DTR}$ low)

NOTES

*The transmitter is disabled immediately. The receiver is disabled but will first complete receiving a byte in process of being received.

**A break is transmitted only after the end of a character stream. If the Transmit Data Register contains a character, the break is not transmitted.

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. $\overline{DTR}$ also enables and disables the transmitter and receiver.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 disables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware reset ($\overline{RES}$)**
–	–	–	0	0	0	0	0	**Program reset**

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

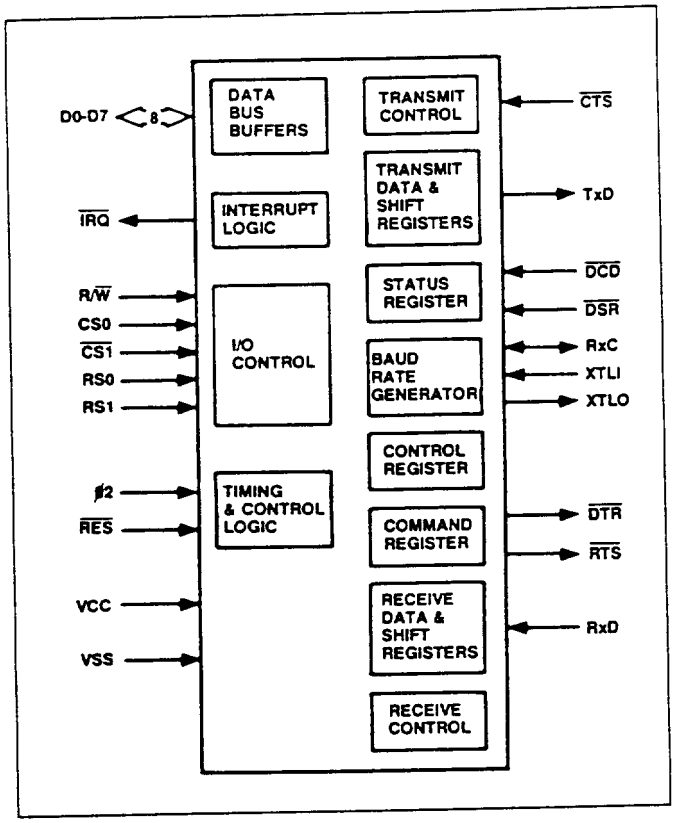


Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset ($\overline{RES}$)

During system initialization a low on the $\overline{RES}$ input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the transmitter Empty bit, which is set. $\overline{RES}$ must be held low for one Ø2 clock cycle for a reset to occur.

Input Clock (Ø2)

The input clock is the system Ø2 clock and clocks all data transfers between the system microprocessor and the ACIA.

NOTE: The specified maximum cycle time for the signal on this input is 40 μs. This specification must be observed to prevent loss of data.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor controls the direction of data transfers A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the commmon $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select decoding.

Table 1. ACIA Register Selection

RS1	RS0	Register Operation	
		R/$\overline{W}$ = Low	R/$\overline{W}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can be both read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset ($\overline{RES}$); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to a series mode external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial nonreturn-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or by an external clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is determined by the programmed baud rate or by an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

RxC is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output pin controls the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

Clear to Send ($\overline{CTS}$)

The $\overline{CTS}$ input pin controls the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

Data Terminal Ready ($\overline{DTR}$)

This output pin indicates the status of the ACIA to the modem A low on $\overline{DTR}$ indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect ($\overline{DCD}$)

The $\overline{DCD}$ input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

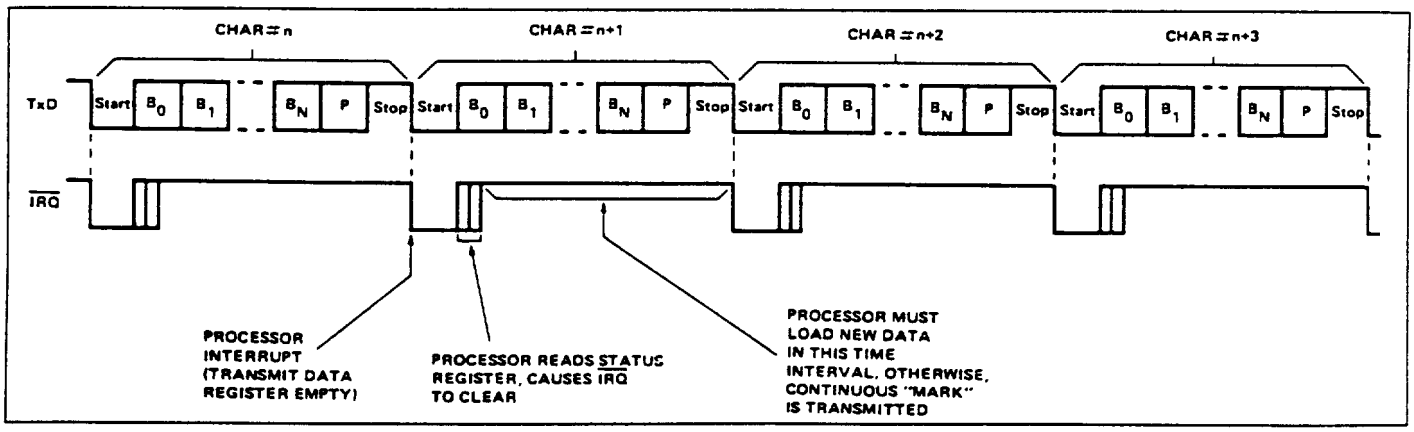


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about $^{9}/_{16}$ point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

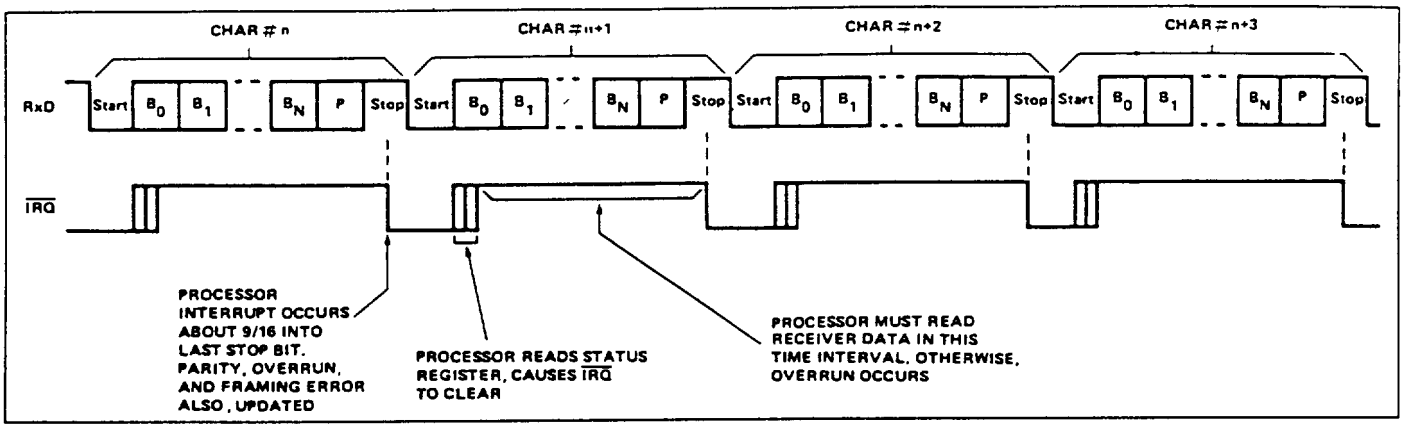


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

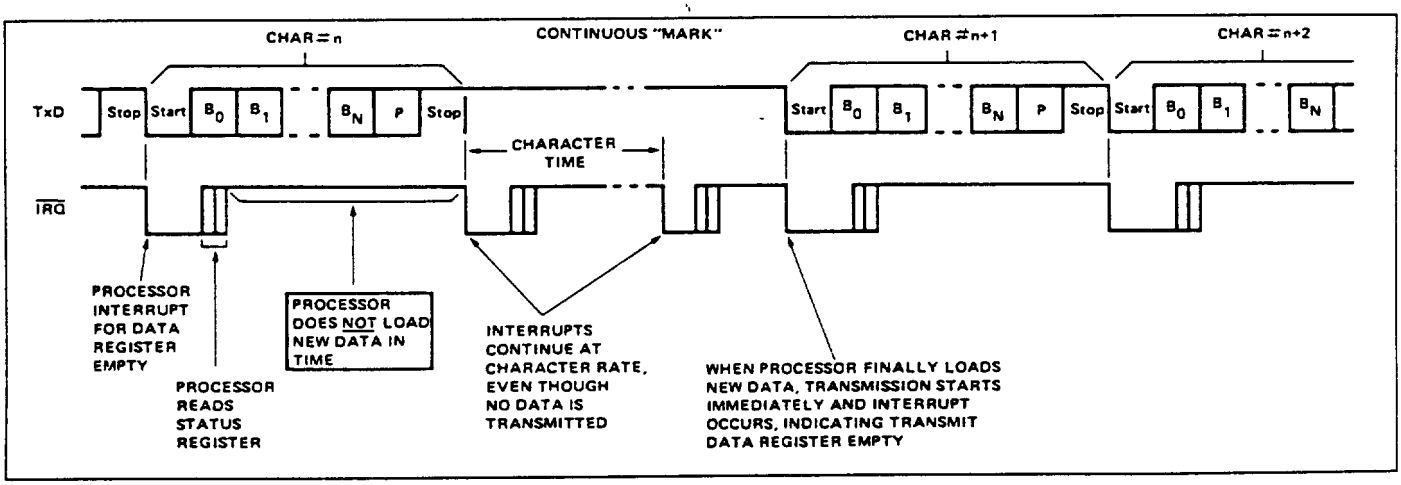


Figure 7. Transmit Data Register Not Loaded by Processor

$\overline{CTS}$ is the Clear-to-Send Signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the FALSE (high) state. $\overline{CTS}$ is a transmit control line only, and has no effect on the R6551 Receiver Operation. Figure 8 shows the timing relationship for this operation

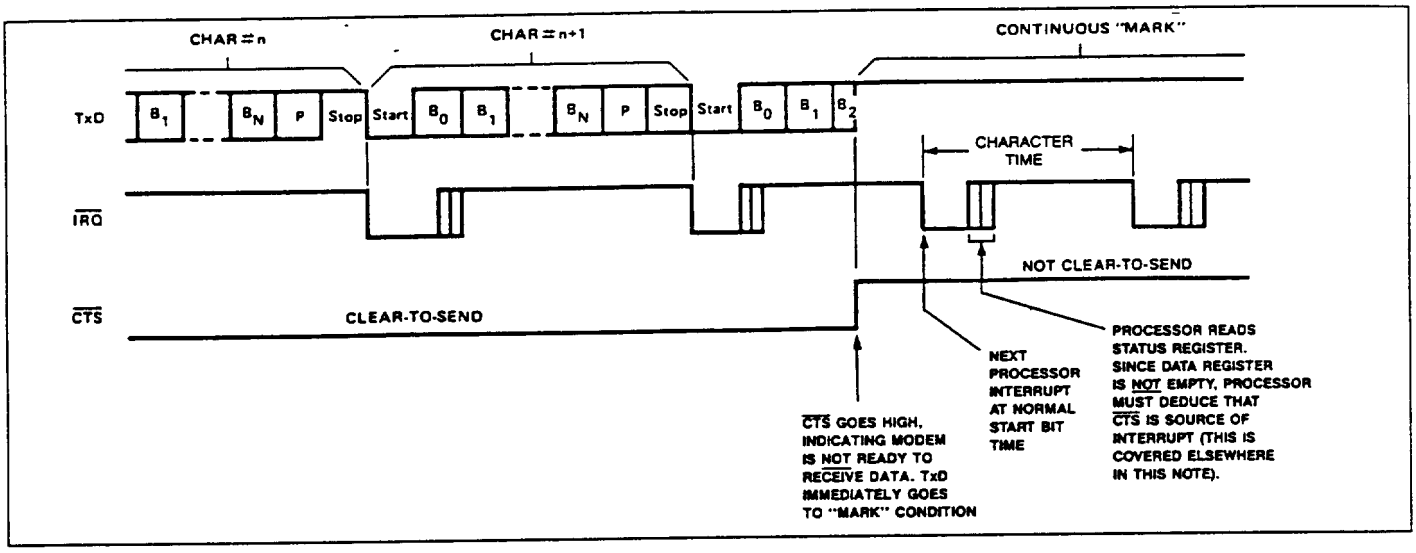


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver data Register in the allocated time, then, when the next interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all fol'owing data is lost. Figure 9 shows the timing relationship for this mode.

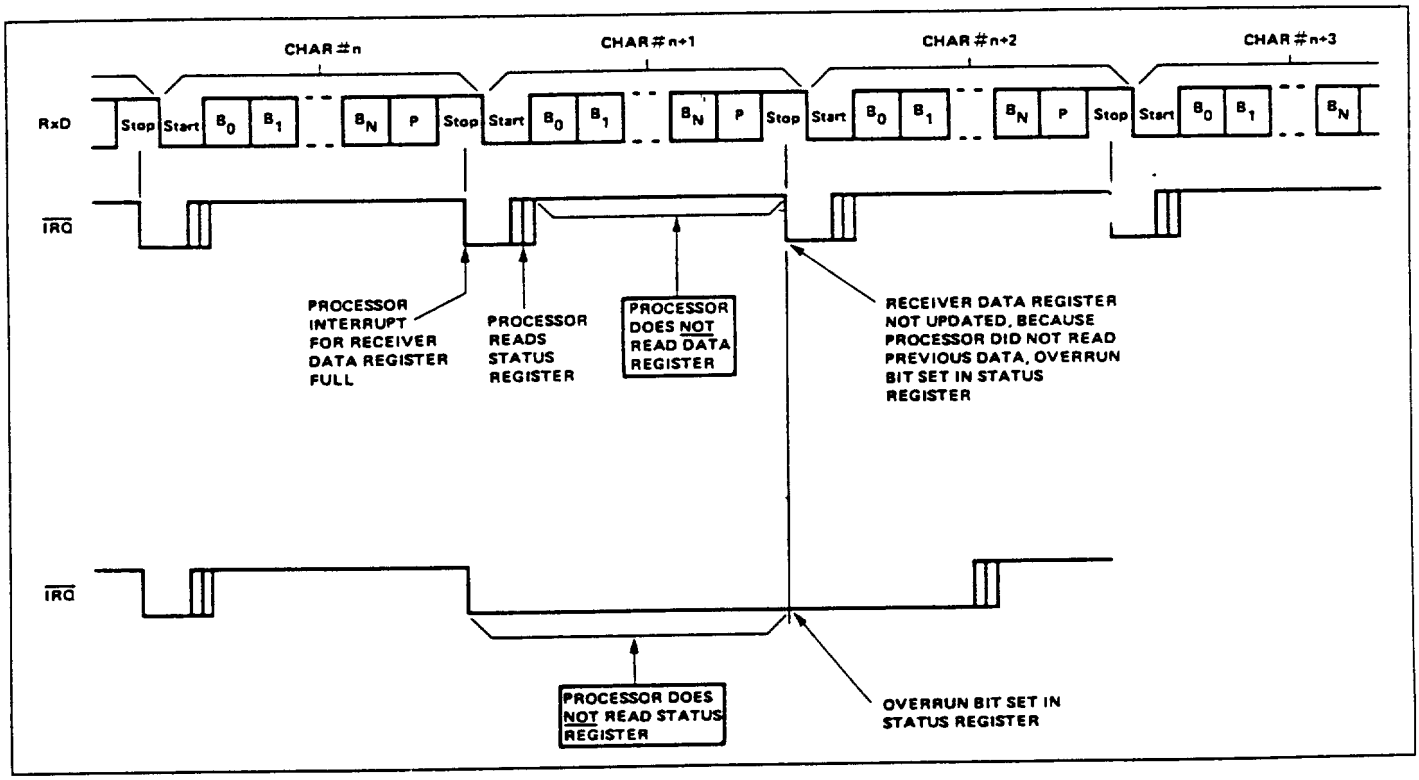


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time, as shown in Figure 10

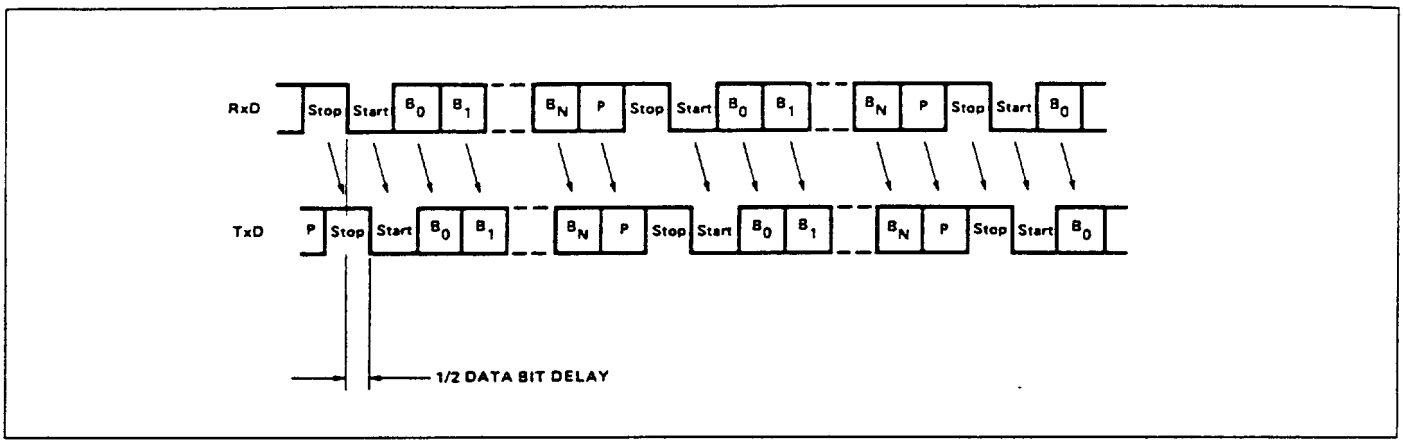


Figure 10. Echo Mode Timing

Effect of $\overline{CTS}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{CTS}$, however, the Transmitter is affected when $\overline{CTS}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that the Receiver Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

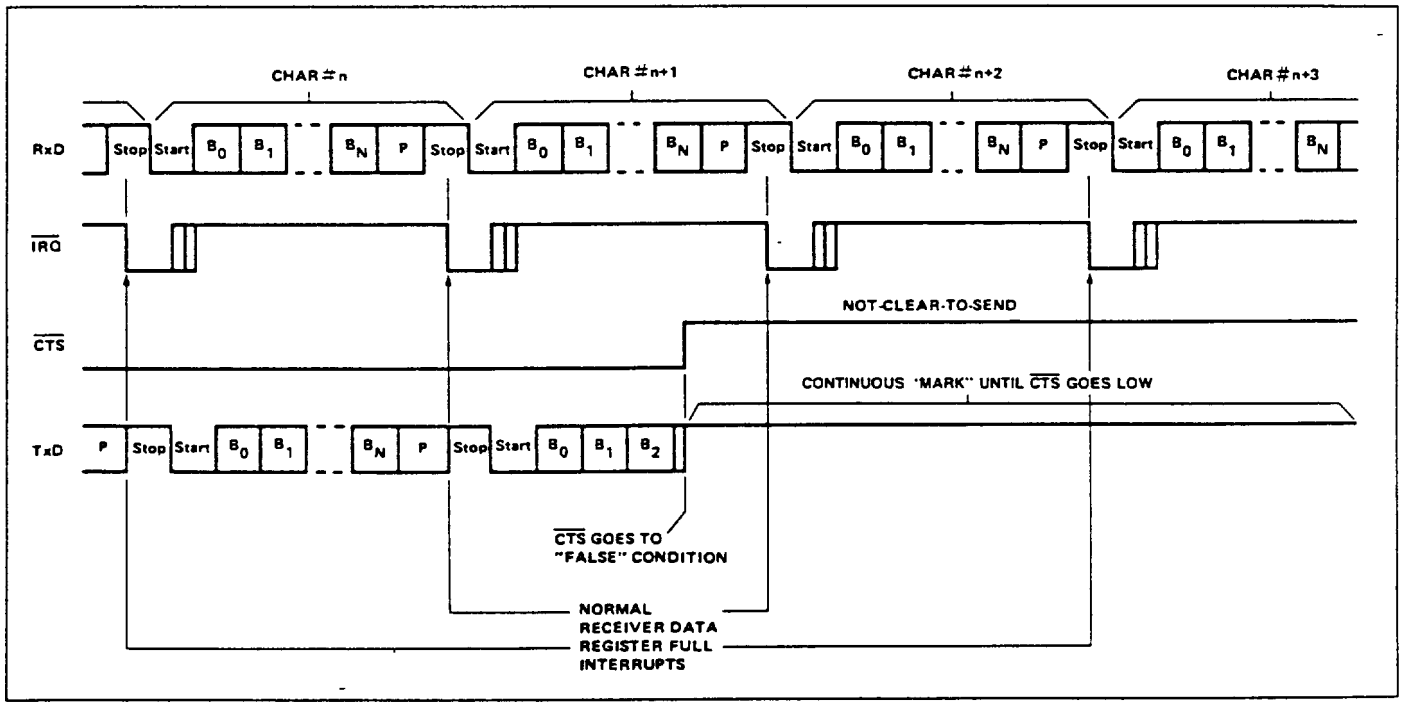


Figure 11. Effect of $\overline{CTS}$ on Echo Mode

Overrun in Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

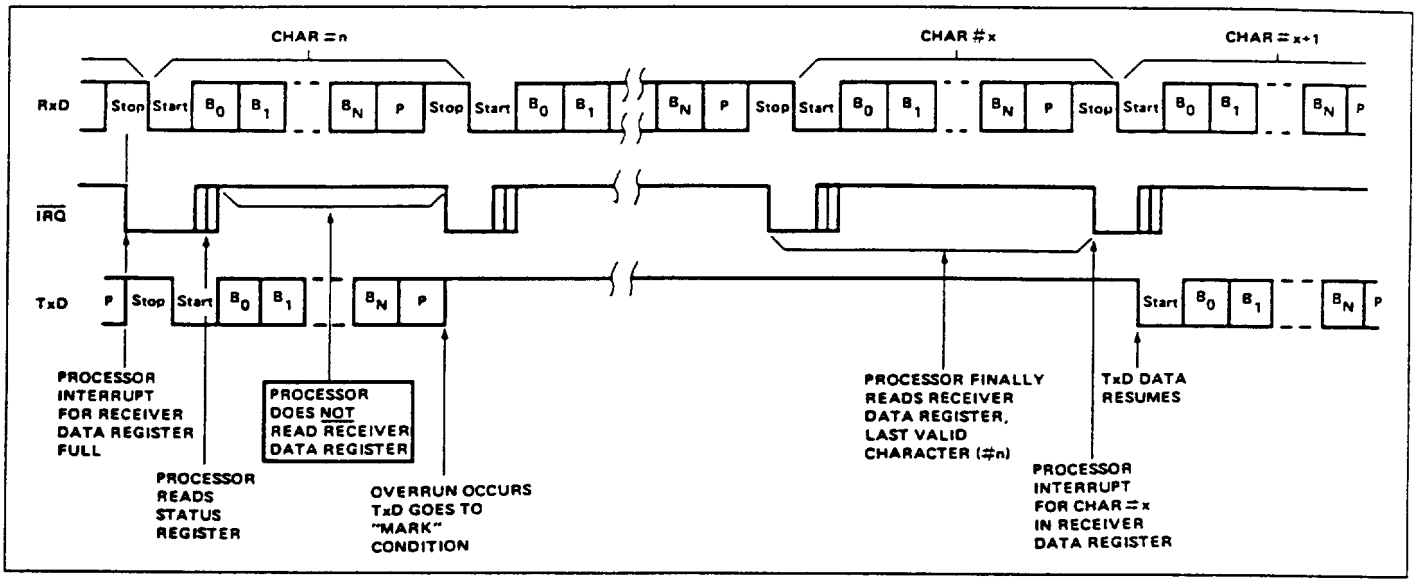


Figure 12. Overrun in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 1 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to $\overline{IRQ}$, generated by RDRF, the Status Register can also be checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

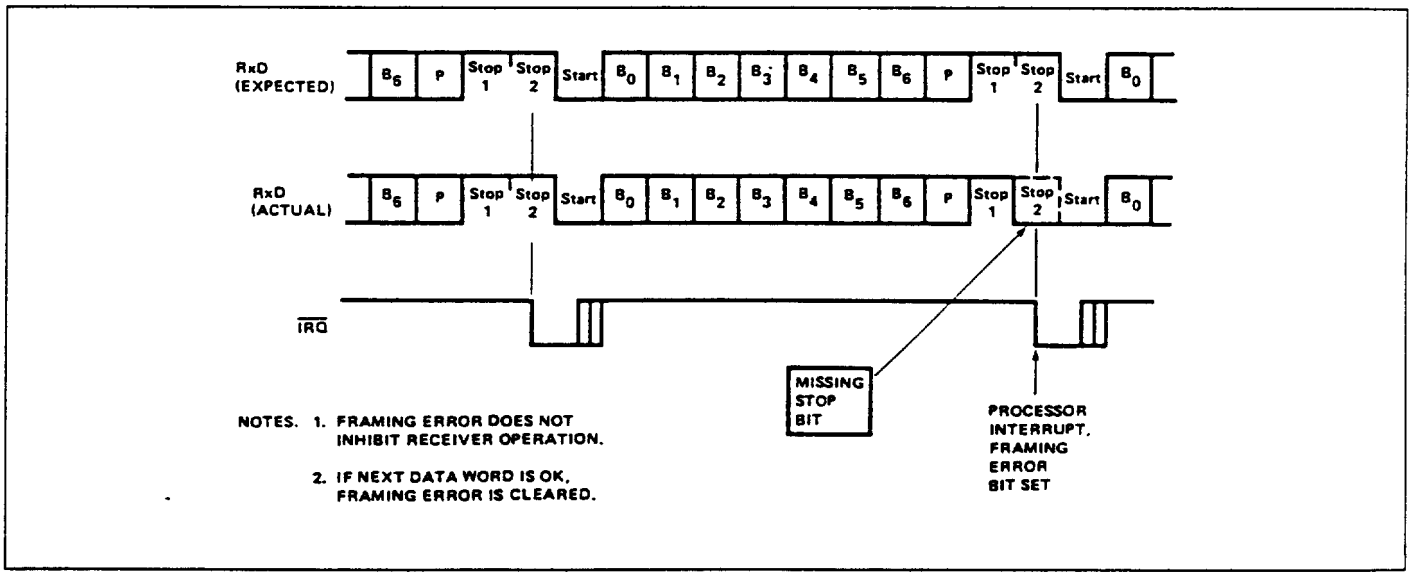


Figure 13. Framing Error

Effect of $\overline{DCD}$ on Receiver

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier Normally, when this occurs, the modem will stop transmitting data some time later The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another $\overline{IRQ}$ occurs (see Figure 14).

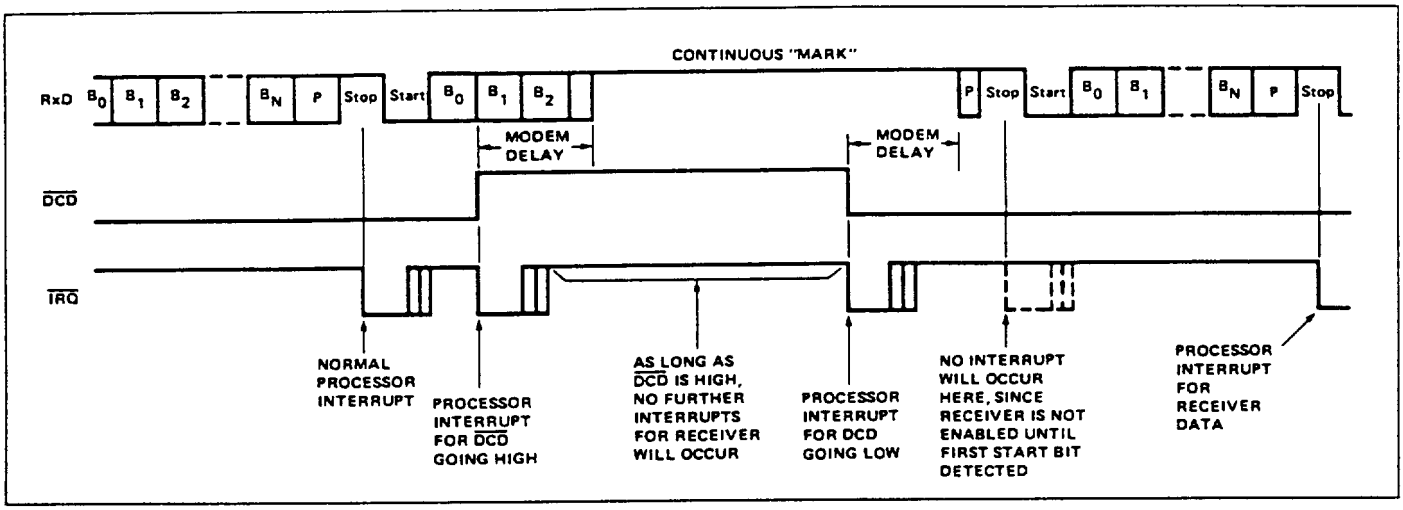


Figure 14. Effect of DCD on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode

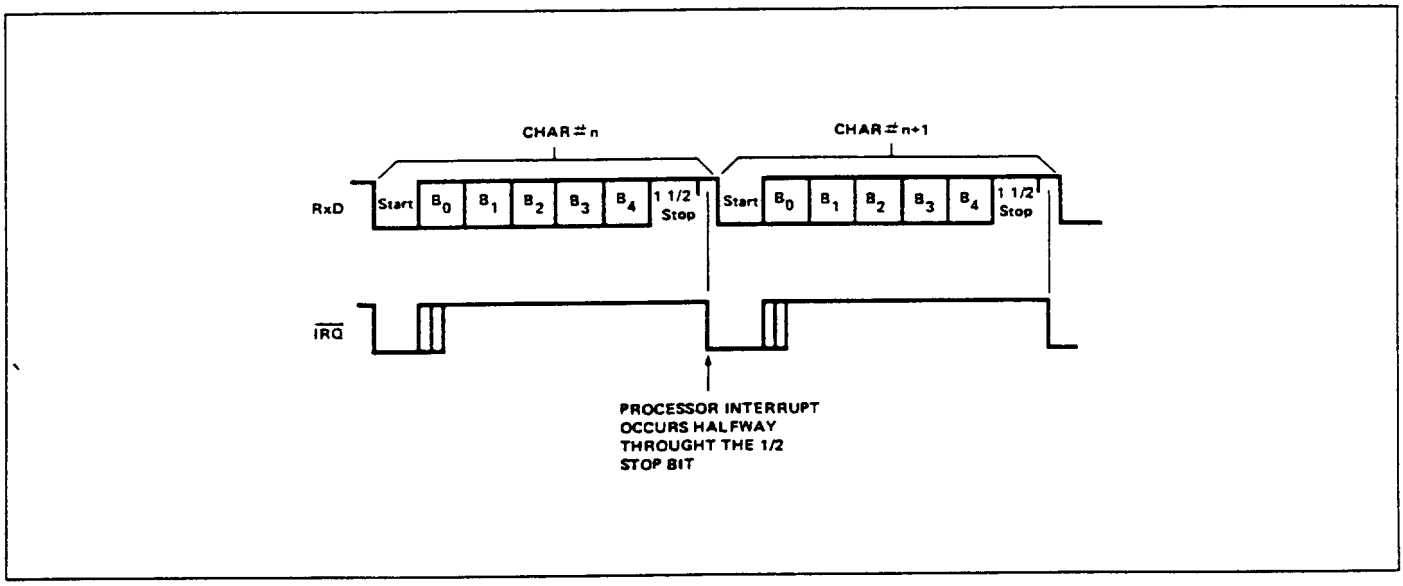


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

Note

If, while operating in the Transmit Continuous "BREAK" mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "MARK" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

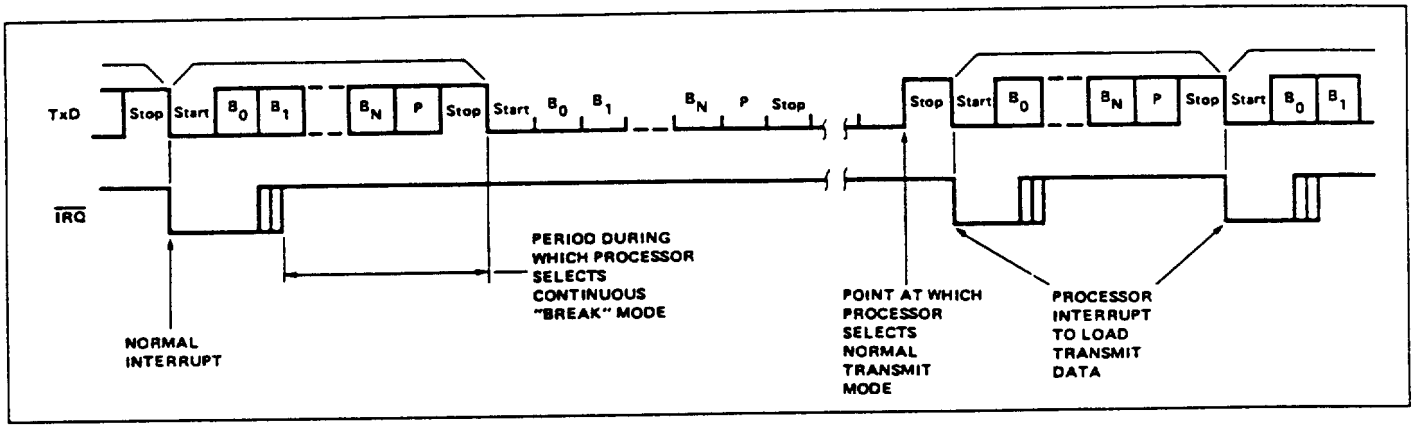


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17 shows the timing relationship for continuous "BREAK" characters.

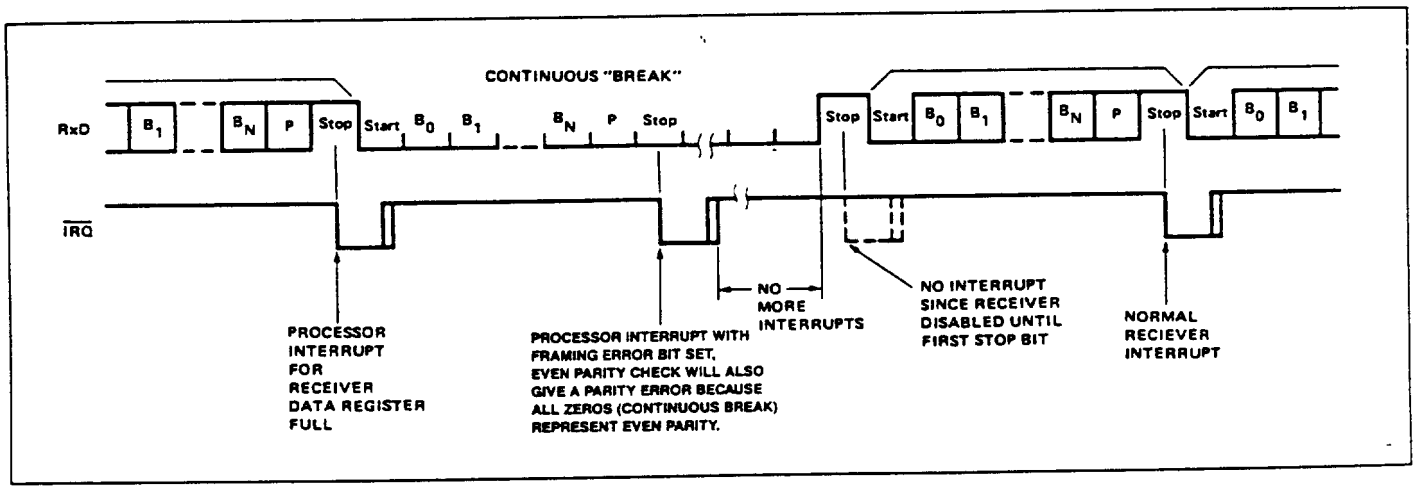


Figure 17. Receive Continuous "BREAK"

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ (Bit 7) in the data read from the Status Register

   If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above conditions exist, then $\overline{CTS}$ must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS1 low and RS0 high. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.

2. The $\overline{DTR}$ line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition

4 $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur

5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes low.

2. If Bit 0 of Command Register ($\overline{DTR}$) is 0 (disabled), then:

   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first

3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.

4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.

5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit time to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. $\overline{DCD}$ andd $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected) If unused, they must be terminated to GND.

CRYSTAL/CLOCK CONSIDERATIONS

CLOCK OSCILLATOR

The on-chip oscillator is designed for a series resonant crystal connected between XTLI and XTLO pins (Figure 18).

A series resonant crystal is specified by the series resistance (R_s) at its series resonant frequency. For proper oscillator operation, the selected series resonant crystal should have a series resistance less than 400 ohms.

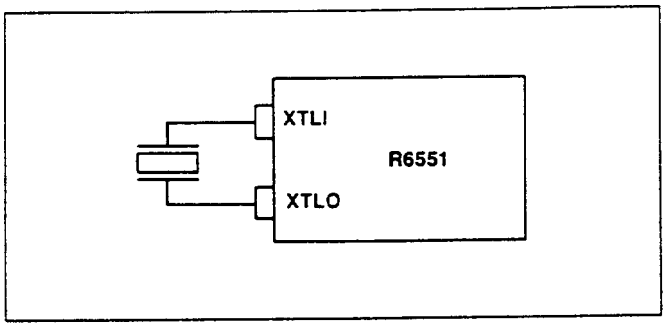


Figure 18. Internal Clock Connection

EXTERNAL CLOCK

The XTLI input may be used as an external clock input (Figure 19) For this implementation, a times 16 clock is input on XTLI and XTLO is left open.

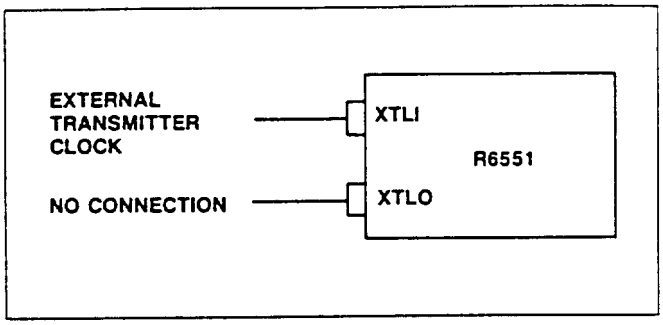


Figure 19. External Clock Connection

BAUD RATE GENERATION

DIVISORS

The internal counter/divider circuit generates appropriate divisors to produce standard baud rates when a 1.8432 MHz crystal is connected between XTLI and XTLO. Control Register bits 0-3 select the divisor for a particular bit rate as shown in Table 2.

GENERATING NON-STANDARD BAUD RATES

By using a different crystal, non-standard baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits 3 2 1 0	Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (F)
0 0 0 0	No Divisor Selected	16 x External Clock at Pin RxC	16 x External Clock at Pin RxC
0 0 0 1	36,864	1.8432 x 10^6 / 36,864 = 50	F / 36,864
0 0 1 0	24,576	1.8432 x 10^6 / 24,576 = 75	F / 24,576
0 0 1 1	16,769	1.8432 x 10^6 / 16,769 = 109.92	F / 16,769
0 1 0 0	13,704	1.8432 x 10^6 / 13,704 = 134.51	F / 13,704
0 1 0 1	12,288	1.8432 x 10^6 / 12,288 = 150	F / 12,288
0 1 1 0	6,144	1.8432 x 10^6 / 6,144 = 300	F / 6,144
0 1 1 1	3,072	1.8432 x 10^6 / 3,072 = 600	F / 3,072
1 0 0 0	1,536	1.8432 x 10^6 / 1,536 = 1,200	F / 1,536
1 0 0 1	1,024	1.8432 x 10^6 / 1,024 = 1,800	F / 1,024
1 0 1 0	768	1.8432 x 10^6 / 768 = 2,400	F / 768
1 0 1 1	512	1.8432 x 10^6 / 512 = 3,600	F / 512
1 1 0 0	384	1.8432 x 10^6 / 384 = 4,800	F / 384
1 1 0 1	256	1.8432 x 10^6 / 256 = 7,200	F / 256
1 1 1 0	192	1.8432 x 10^6 / 192 = 9,600	F / 192
1 1 1 1	96	1.8432 x 10^6 / 96 = 19,200	F / 96

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an ACIA is shown in Figure 20

It may be desirable to include in the system a facility for local loop-back testing.

In loop-back testing from the point of view of the processor, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry Figure 21 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables outputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs (i.e TxD to RxD, $\overline{DTR}$ to $\overline{DCD}$, $\overline{RTS}$ to $\overline{CTS}$)

LLB may be tied to a peripheral control pin (from an R6520 or R6522, for example) to provide processor control of local loop-back operation In this way, the processor can easily perform local loop-back diagnostic testing

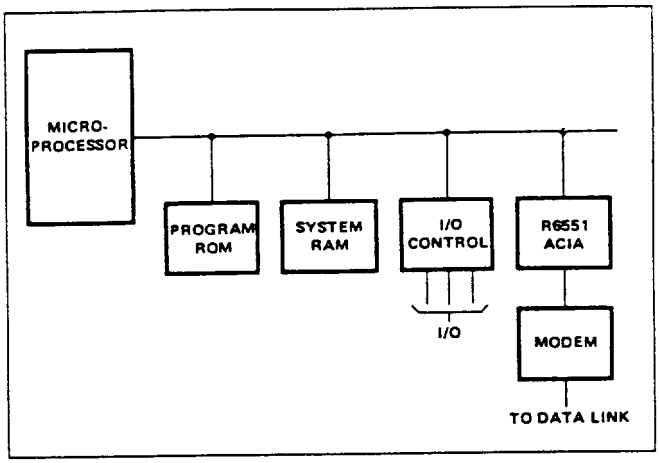


Figure 20. Simplified System Diagram

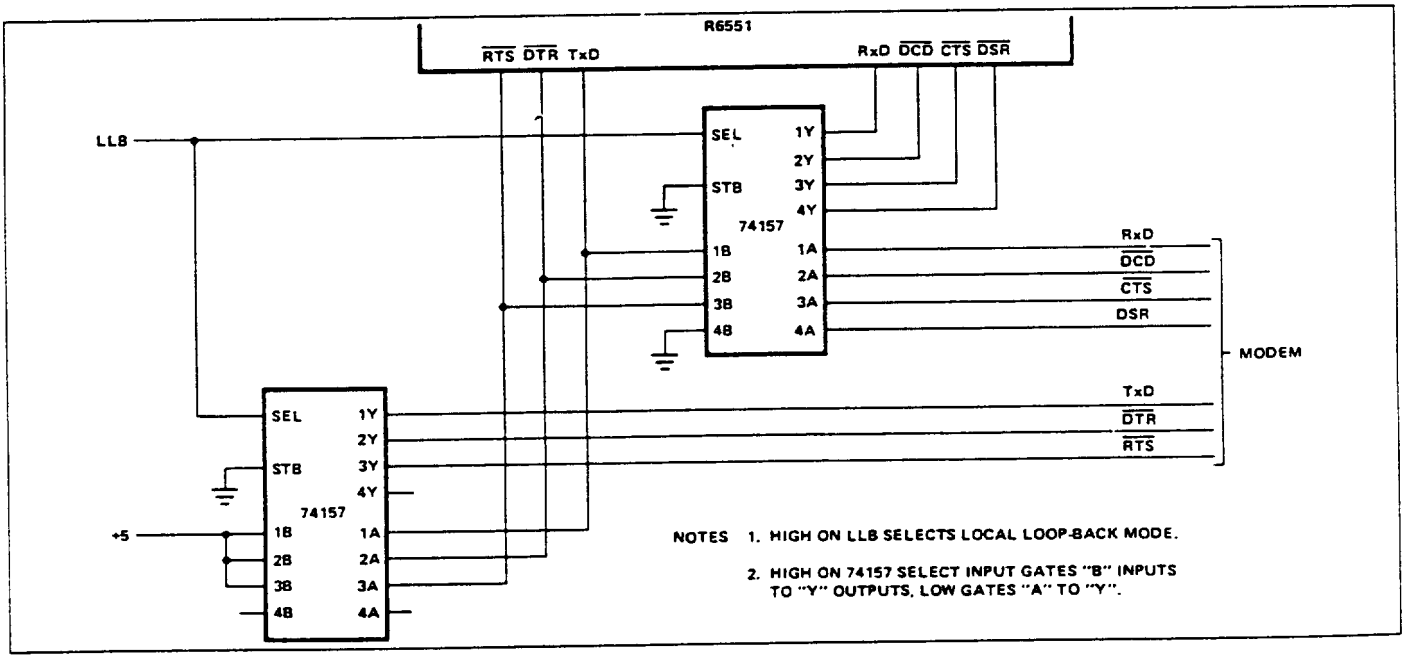


Figure 21. Loop-Back Circuit Schematic

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{IRQ}$ generation are shown in Figures 22, 23 and 24, respectively. The corresponding timing characteristics are listed in the Table 3

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
RTS Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns
Load Capacitance $\overline{DTR}$, RTS TxD	C_L	 — —	 130 30	 — —	 130 30	 pF pF

Notes:
(t_R, t_F = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

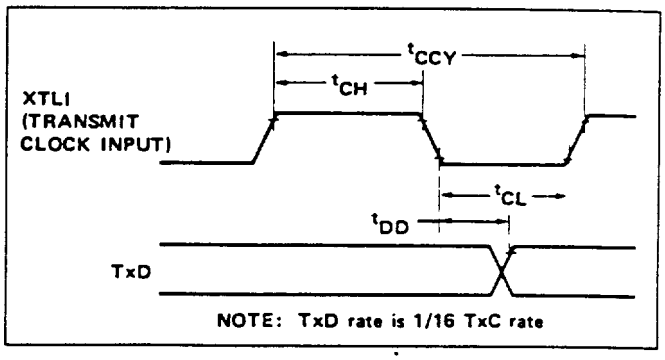


Figure 22. Transmit Timing with External Clock

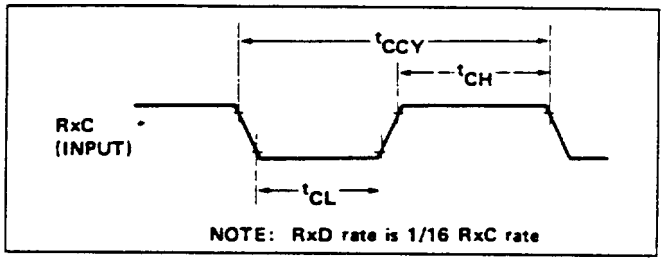


Figure 23. Receive External Clock Timing

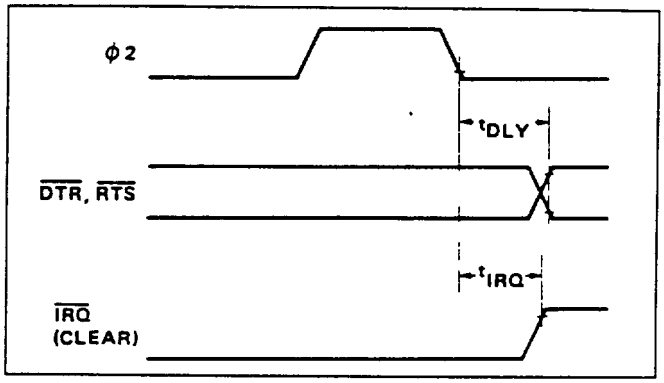


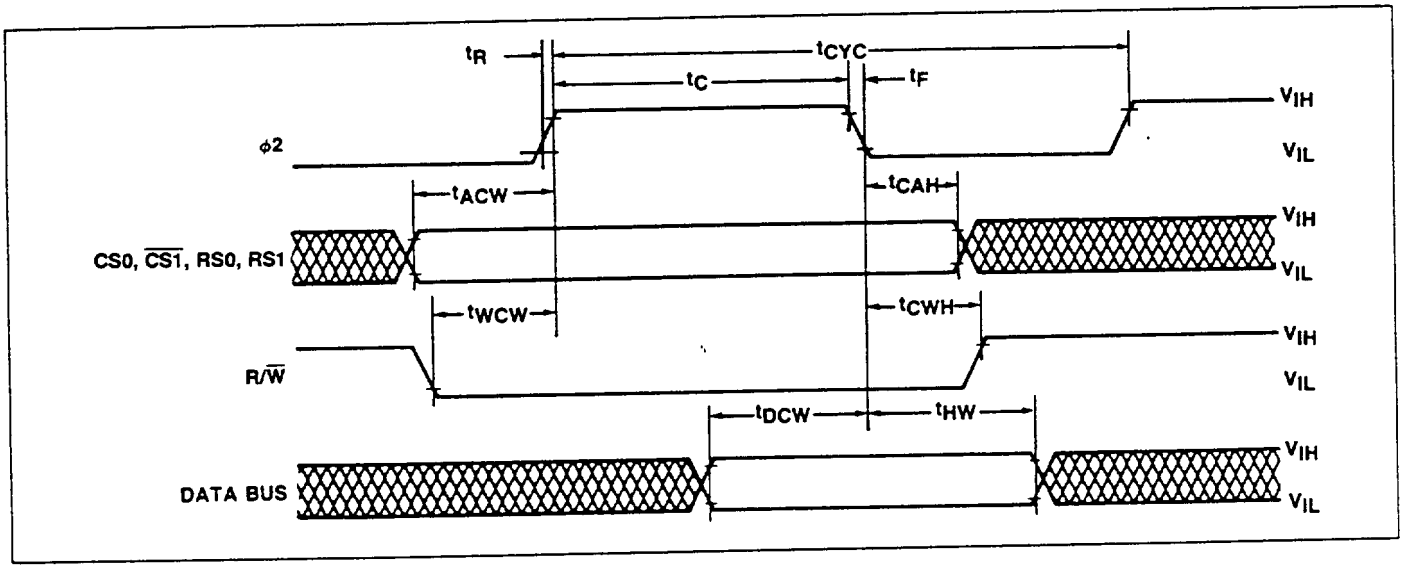
Figure 24. Interrupt and Output Timing

AC CHARACTERISTICS

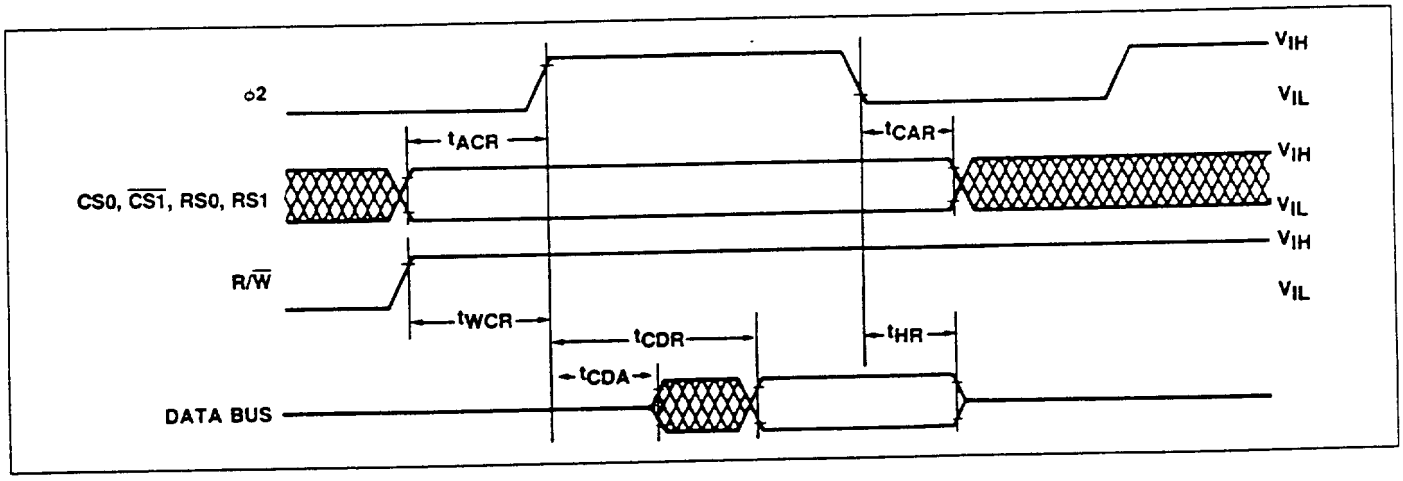
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1 0	40	0.5	40	μs
ø2 Pulse Width	t_C	400	—	200	—	ns
Address Set-Up Time	t_{ACW}, t_{ACR}	120	—	70	—	ns
Address Hold Time	t_{CAH}, t_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}, t_{WCR}	120	—	70	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	150	—	60	—	ns
Data Bus Hold Time	t_{HW}	20	—	20	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	150	ns
Read Hold Time	t_{HR}	20	—	20	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	40	—	ns

Notes: 1. t_R and t_F = 10 to 30 ns.
2. D0-D7 load capacitance = 130 pF
3. Timing measurements are referenced to/from a low of 0 8 volts and a high of 2.0 volts.



Write Timing Diagram



Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0 3 to V_{CC}	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC}	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

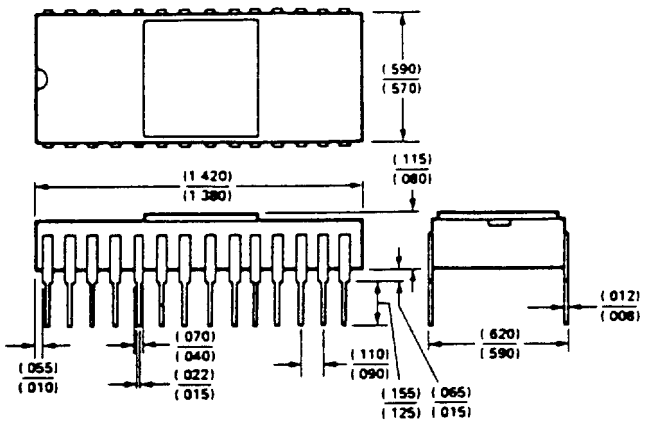
DC CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

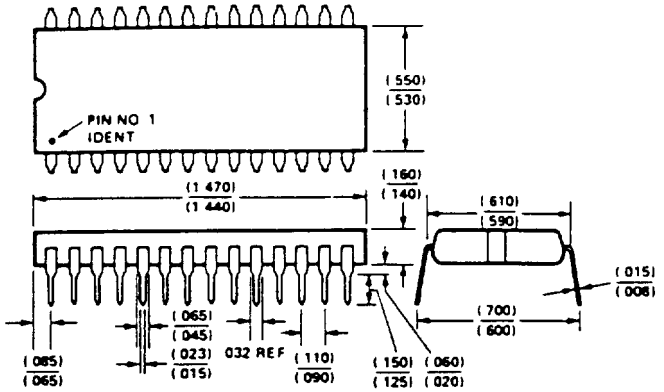
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTLI and XTLO XTLI and XTLO	V_{IH}	 2.0 2.4	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage Except XTLI and XTLO XTLI and XTLO	V_{IL}	 V_{SS} V_{SS}	 — —	 0.8 0.4	V	
Input Leakage Current Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, CS1, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$	I_{IN}	—	—	2.5	μA	V_{IN} = 0V to 5V V_{CC} = 0V
Input Leakage Current for High Impedance (Three State Off) D0–D7	I_{TSI}	—	—	±10.0	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	V_{OH}	2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4 75V
Output Low Voltage D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	V_{OL}	—	—	0.4	V	V_{CC} = 4 75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	I_{OH}	−100	—	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking) D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	I_{OL}	1.6	—	—	mA	V_{OL} = 0 4V
Output Leakage Current (off state) $\overline{IRQ}$	I_{OFF}	—	—	10.0	μA	V_{OUT} = 5V
Clock Capacitance (Ø2)	C_{CLK}	—	—	20	pF	V_{CC} = 5V V_{IN} = 0V f = 1 MHz T_A = 25°C
Input Capacitance except Ø2, XTLI, XTLO	C_{IN}	—	—	10	pF	
Output Capacitance	C_{OUT}	—	—	10	pF	
Power Dissipation	P_D	—	170	300	mW	T_A = 0°C

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



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